Remarks

Reconsideration and further examination is respectfully requested. Claims 1-25 were originally presented for examination. Claims 1, 3-10, 12-17 and 19-25 were amended in a reply to a First Office Action. New claims 26 and 27 have been added. Claims 1-27 are presented for further examination.

The Examiner has stated that the title of the invention is not sufficiently descriptive. The title has been amended to reflect SPICE to VERILOG translation and a design method using SPICE to VERILOG and VERILOG TO SPICE translation.

The Examiner objected to the abstract as not properly disclosing the substance of the applicant's invention. A replacement abstract has been provided to address this deficiency.

The Examiner has asserted that figures 1, 4, and 5 in the drawings should be labeled as prior art. Figure 4 depicts a design flow in which a first part of a design is implemented using Verilog and a second part of the design is implemented using SPICE. The SPICE is converted to Verilog, allowing simulation of both parts of the design using Verilog. Naun discloses model validation between SPICE and Verilog, but does not disclose or suggest a design flow as depicted in figure 4. Figure 5 depicts steps employed to translate a SPICE netlist to Verilog. Embodiments of the present invention employ hierarchical constructs (such as XINV for inverter) that are not disclosed or suggested by Naun and therefore step 510 of figure 5 is not disclosed or suggested by the cited art. With regard to figure 1, Rostoker (US 6,470,482) discloses design employing VHDL or graphical selection and interconnection of predefined components. Custom logic design is disclosed but custom circuit design and SPICE are not disclosed. Haddad (US 6,526,562) discloses custom standard cells, but does not disclose custom logic that is not a standard cell, such as a hard macro, for example. While the method depicted in figure 1 may include methods disclosed in Rostoker and Haddad, it is also not constrained to such methods, including standard cell design environments. Hence, applicant has not amended figure 1.

Claim Rejections

The Examiner rejected claims 10-16 under 35 U.S.C. 102(b) as being anticipated by a paper entitled Automatic Functional Model Validation Between Spice and Verilog.

In brief, Naum discloses a method for validating a Verilog model for a SPICE design. The SPICE model of Naum is a "flat" model in that it comprises a list of P and N transistors but contains no hierarchy, making it difficult to understand the function or functions provided. Similarly, the translated Verilog file lacks hierarchy that also makes it difficult to understand the function or functions provided.

In contrast, embodiments of the present invention employ one or more circuit elements that define the function or functions provided, as recited in claim 10 that includes the element of "a SPICE file comprising a subcircuit name identified by a ".SUBCKT" heading, at least one input signal name, at least one circuit element, at least one discrete circuit element description, an output signal name, and a .ENDS statement". Naum's SPICE files only employ discrete circuit elements and does not contain a circuit element, such as an AND gate, inverter, or OR gate, for example. Advantageously, translation of SPICE to Verilog at the circuit element level can maintain the hierarchy and signal name associations of the SPICE design in the translated Verilog file.

Applicant therefore respectfully asserts that the rejection of claims 10-16 under 35 U.S.C. 102(b) as being anticipated by Michael Naum et al is improper because the cited art does not teach or suggest all of the claim elements. Specifically, Naum does not teach or suggest "a SPICE file comprising" ... "at least one circuit element" ... "translating said at least one circuit element in said SPICE file to Verilog format" as recited in claim 10. Naun does not recognize the benefit of maintaining hierarchy and does not teach or suggest a corresponding method.

Conclusion

In view of the above stated reasons, this application is now considered to be in condition for allowance and such action as earnestly solicited.

Dated this 23rd day of September 2003.

Respectfully submitted,

William W. Cochran
Attorney for Applicant
Reg. No. 26,652
The Law Offices of William W. Cochran, LLC
3555 Stanford Road, Suite 230
Fort Collins, CO 80525
Phone: (970) 377-6363
Fax: (970) 207-1985